Spartan-6 FPGA GTP Transceiver Signal Integrity Simulation Kit User Guide

For Mentor Graphics HyperLynx

UG396 (v1.0) June 10, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/10/10	1.0	Initial Xilinx release.

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About This Guide

This guide describes the Spartan®-6 FPGA GTP Transceiver Signal Integrity Simulation (SIS) Kit for Mentor Graphics HyperLynx.

Guide Contents

This user guide contains this chapter and appendices:

- Chapter 1, Spartan-6 FPGA GTP Transceiver Signal Integrity Simulation Kit, explains installation, configuration, and use of the HyperLynx software to simulate Spartan-6 FPGA GTP transceivers.
- Appendix A, Frequently Asked Questions, explains HyperLynx error messages.
- Appendix B, HSPICE and HyperLynx/Eldo Correlation Results, contains the correlation results and explains how they were derived.

Additional Support Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Spartan-6 FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section Additional Support Resources for details. Refer to Overview, page 7 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

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Chapter 1

Spartan-6 FPGA GTP Transceiver Signal Integrity Simulation Kit

Introduction

The Spartan®-6 FPGA GTP Transceiver Signal Integrity Simulation (SIS) Kit for Mentor Graphics HyperLynx provides a simulation environment for evaluating channel designs for Spartan-6 FPGA GTP transceivers. This document explains how to install the SIS kit and associated files, gives an overview of the SIS kit file hierarchy, and describes the steps for getting started with simulations. The appendices describe how the HyperLynx and Eldo simulation results are correlated with the HSPICE simulations. Results are documented with waveform plots.

Additional information on the models, ports, and options is available in UG386, *Spartan-6 FPGA GTP Transceivers User Guide*.

Release Notes for the GTP Transceiver SIS Kit

Table 1-1 shows the UG396 document version and the associated Spartan-6 FPGA GTP Transceiver SIS Kit version.

Table 1-1: **Document and SIS Kit Version Correlation**

UG396 Version	SIS Kit Version
1.0	1.0

Installation and Requirements

The software requirements and the installation instructions for the Spartan-6 FPGA GTP Transceiver SIS Kit are provided in this section.

SIS Kit Version 1.0

The requirements for the GTP Transceiver SIS Kit are:

- HyperLynx 8.0, build number 433 or later
- Microsoft Windows XP Professional, version 2002, Service Pack 3

To install the GTP Transceiver SIS Kit, follow these steps:

1. Unzip the ZIP file into any directory, provided that the path name does not contain any spaces.

2. To prevent errors or warnings when the project files are moved to a different directory (or computer), replace the path listed on the last line in the PJH files (located in the `HL_projects` subdirectory) with a relative path:

   `INIFILE=.\S6_kit.ini`.

   Note: HyperLynx automatically replaces this relative path with a full path when opening the project. Therefore, this change should be made every time the project is moved or copied to a different location.

3. For better convergence, set ForceFixedStep = 0 under the [SPICE] keyword in the `bsw.ini` file in the HyperLynx Installation directory.

File Hierarchy

The top-level directory into which the ZIP file is unzipped contains several subdirectories. The HyperLynx project files are all located in the `hl_projects` subdirectory. Any example project can be opened by double-clicking on the respective FFS file in Windows Explorer or by starting HyperLynx, going to **File/Open Schematic...**, and then clicking on **Open Linesim File**.

Model files are located in the subcircuits under the top-level project directory.

Subcircuits are referenced by the HyperLynx schematic symbols. The INC files containing the simulation parameters are located under the `testbenches` directory along with the configurator executable programs. There should be no reason to manually modify these files. All modifications are made via the HyperLynx Graphical User Interface.

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Getting Started

The steps in this section must be observed to run simulations:

Opening an Example

The user can double-click on any FFS file in Windows Explorer to start a project in HyperLynx. This user guide uses `GTP_Tx_channel_GTP_Rx` as an example, but this discussion applies to the other testbenches as well. The user can double-click on the `GTP_RefClk.ffs` or the `GTP_Tx_channel_GTP_Rx.ffs` file in the `hl_projects` directory in Windows Explorer to start HyperLynx. Because the latter file is the more complicated testbench, the remaining part of this document discusses that testbench only.

HyperLynx should start without any error or warning messages and look as shown in Figure 1-1.

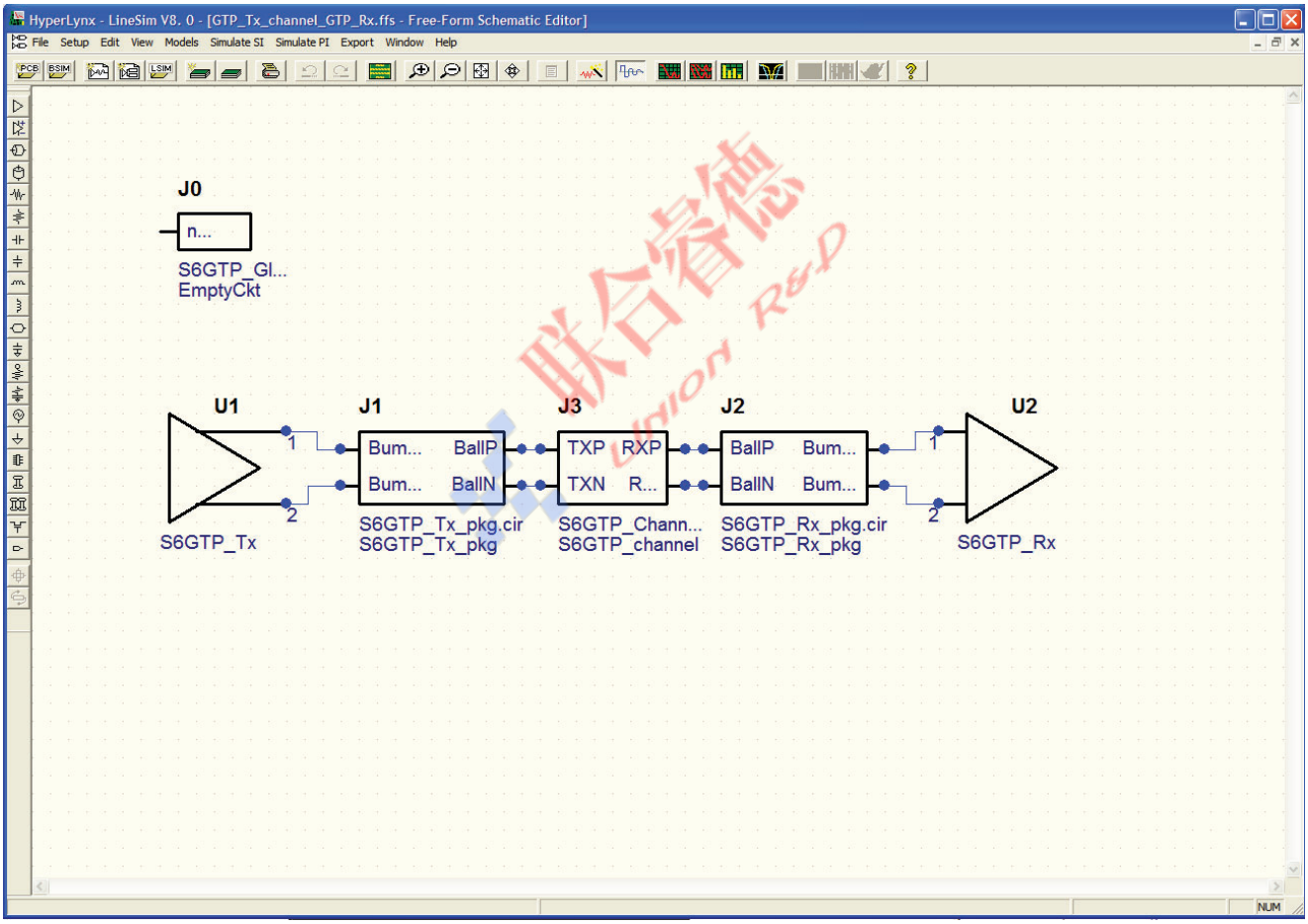

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Figure 1-1: **HyperLynx**

Note: The *J0* symbol must appear unconnected on the schematics screen. This symbol should not be removed from the schematics because it is used to insert global simulation parameters, such as **`.TEMP`** and **`.option compat`** (the HSPICE compatibility switch for Eldo), into the project. These parameters are managed automatically by the configurator programs. Removing *J0* results in incorrect simulations.

Modifying the Driver Settings

1. Double-click on **U1** to open the **Assign Models** dialog box and click the **Configure Model** button, as shown in Figure 1-2.

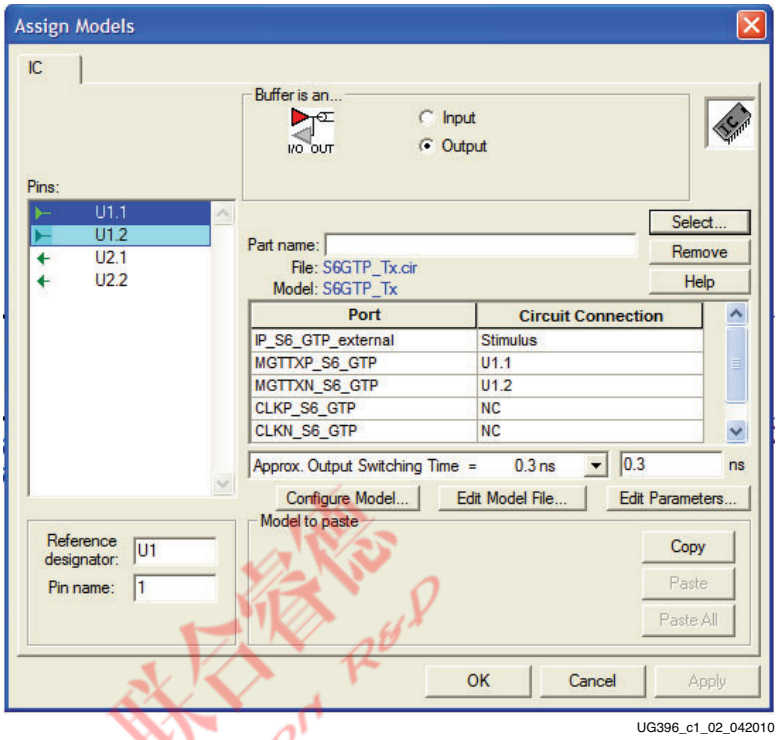

Figure 1-2: **Assign Models**

For more information on the driver settings, refer to UG386, *Spartan-6 FPGA GTP Transceivers User Guide*.

Notes relevant to this step:

- The global simulation temperature setting can be changed in either driver or receiver configurators. However, being a global setting in Eldo, the last change made is applied to the entire circuit, regardless of whether the TX or RX configurator is used to make that change.
- Be sure to click only once, because each click starts a new instance of the configurator. If multiple instances of the configurators are open, close all but one of them by clicking on their **Cancel** buttons.

2. Make the desired changes to any of the parameters, and press the **OK** button to exit. This writes the necessary configuration files for the simulation.

   Note: The frequency of the pulse train or the time of the bit interval specified in the oscilloscope *must* match the Data rate setting in the TX configurator (see Figure 1-3). Each setting must be done explicitly.

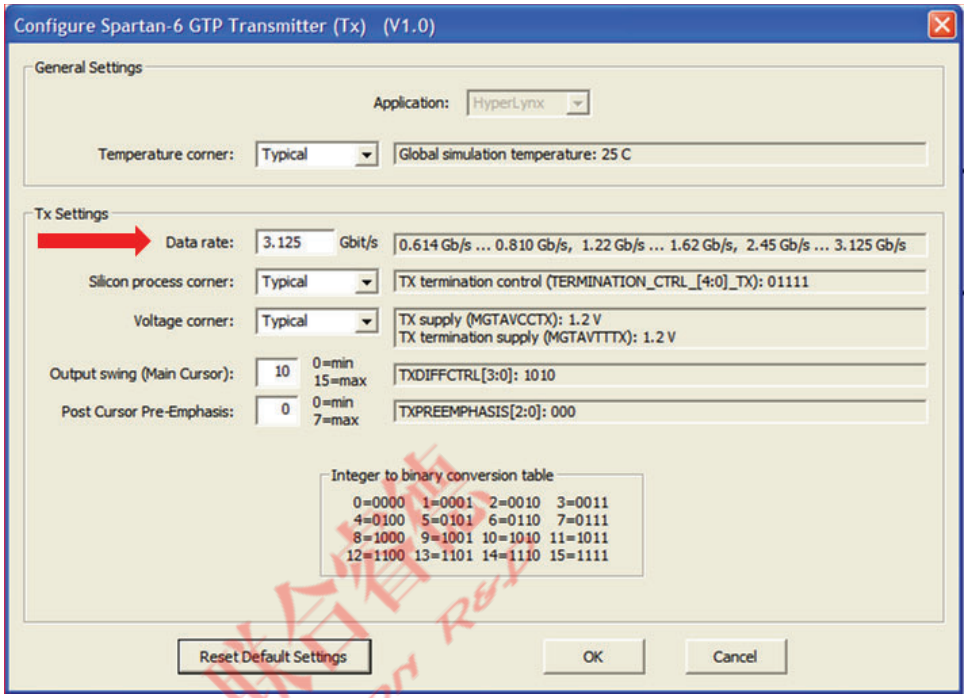

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Figure 1-3: **Configure Spartan-6 FPGA GTP Transmitter**

The setting for the **Approx. Output Switching Time = 0.3 ns** drop-down box shown in Figure 1-4 is meant to be the SPICE driver output (not stimulus) rise or fall time and is used to set the step size and estimate crosstalk effects in the simulation. The value of this parameter can be changed if desired. Relaxing this parameter allows the user to select larger simulation time steps in the **Run Eldo/ADMS Simulation** dialog box, which might result in non-converging simulations.

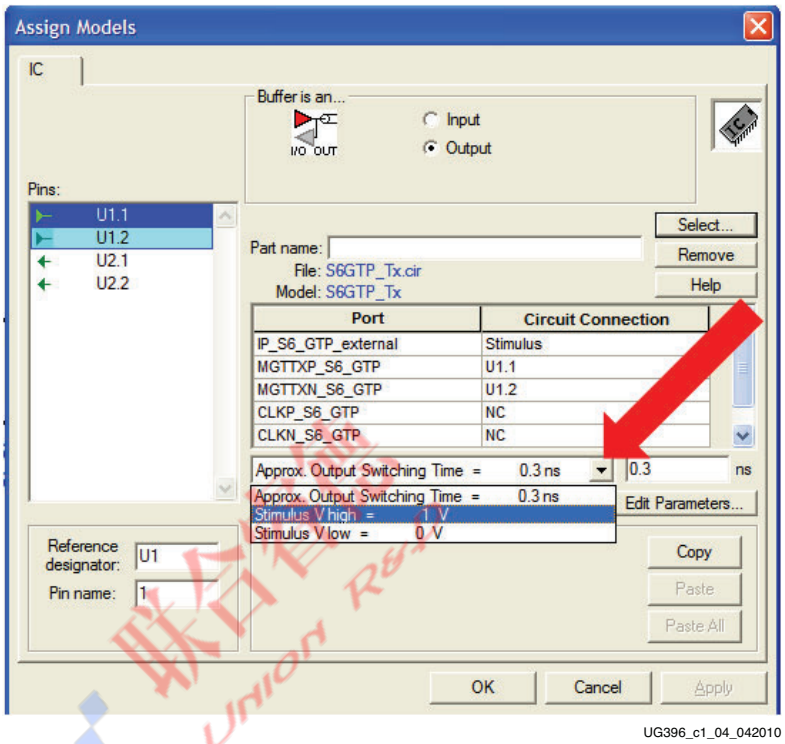

Figure 1-4: **Output Switching Time**

The drop-down box shown in Figure 1-4 has two additional entries for the High and Low voltage levels of the stimulus generated by HyperLynx. Do not modify these numbers because they are closely related to the content of the netlist. The voltage levels in the `GTP_RefClk.ffs` testbench must be set to **`-1V`** for **`Stimulus V low`** and **`+1V`** for **`Stimulus V high`**. In the rest of the testbenches, they should be set to **`0V`** for **`Stimulus V low`** and **`+1V`** for **`Stimulus V high`**.

3. When the desired changes are made, click on the **OK** button to close the **Assign Models** dialog box.

Customizing the Channel Representation

Use the available HyperLynx toolbox to add S-parameter models, transmission lines, vias, and so forth.

The provided example contains an S-parameter model representing a 20-inch microstrip trace with SMA connectors on each side. The board material is FR-4. A custom channel representation can be created using the HyperLynx toolbox to add S-parameter models, transmission lines, vias, and so forth.

Modifying the Receiver Settings

Repeat the steps in Modifying the Driver Settings. Adjust the receiver (**U2**) simulation parameters.

For more information on the driver settings, refer to UG386, *Spartan-6 FPGA GTP Transceivers User Guide*.

Notes relevant to this section:

- The global simulation temperature setting can be changed in either driver or receiver configurators (see Figure 1-5). However, because it is a global setting in Eldo, the last change made is applied to the entire circuit, regardless of whether the TX or RX configurator is used to make that change.
- Be sure to click only once. If multiple instances of the configurators are open, close all but one by clicking their **Cancel** buttons.

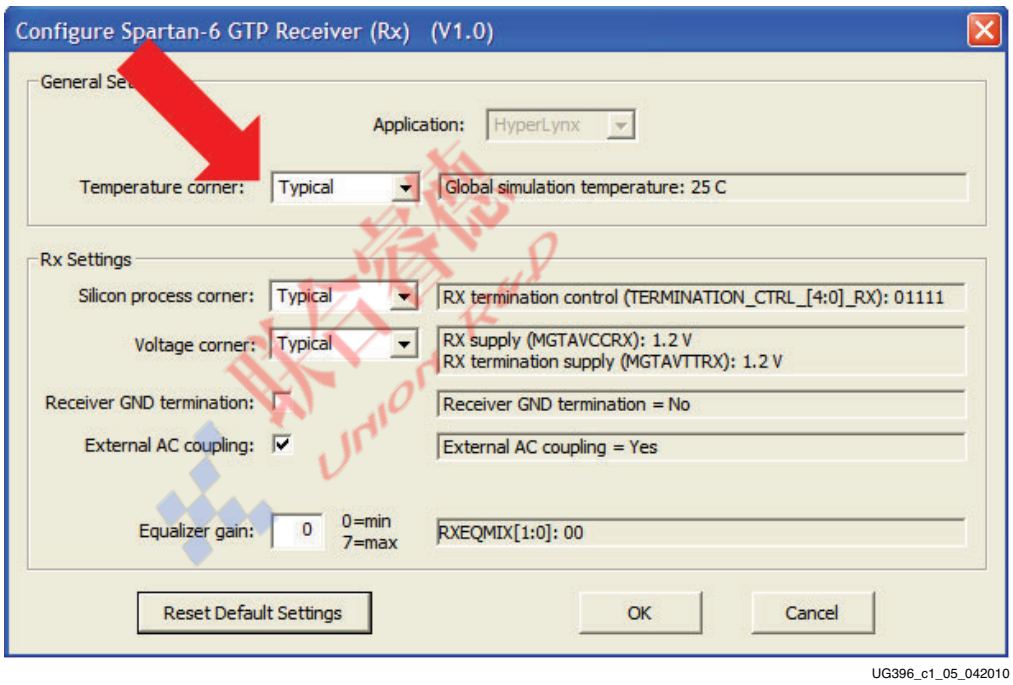

Figure 1-5: **Configure Spartan-6 FPGA Receiver**

Adjusting Simulation Settings

1. Click **Run Interactive Simulation (Oscilloscope)** under the **Simulate** tab.
2. Select the **Eldo/ADMS** radio button under the **Start Simulation** button, as shown in Figure 1-6.

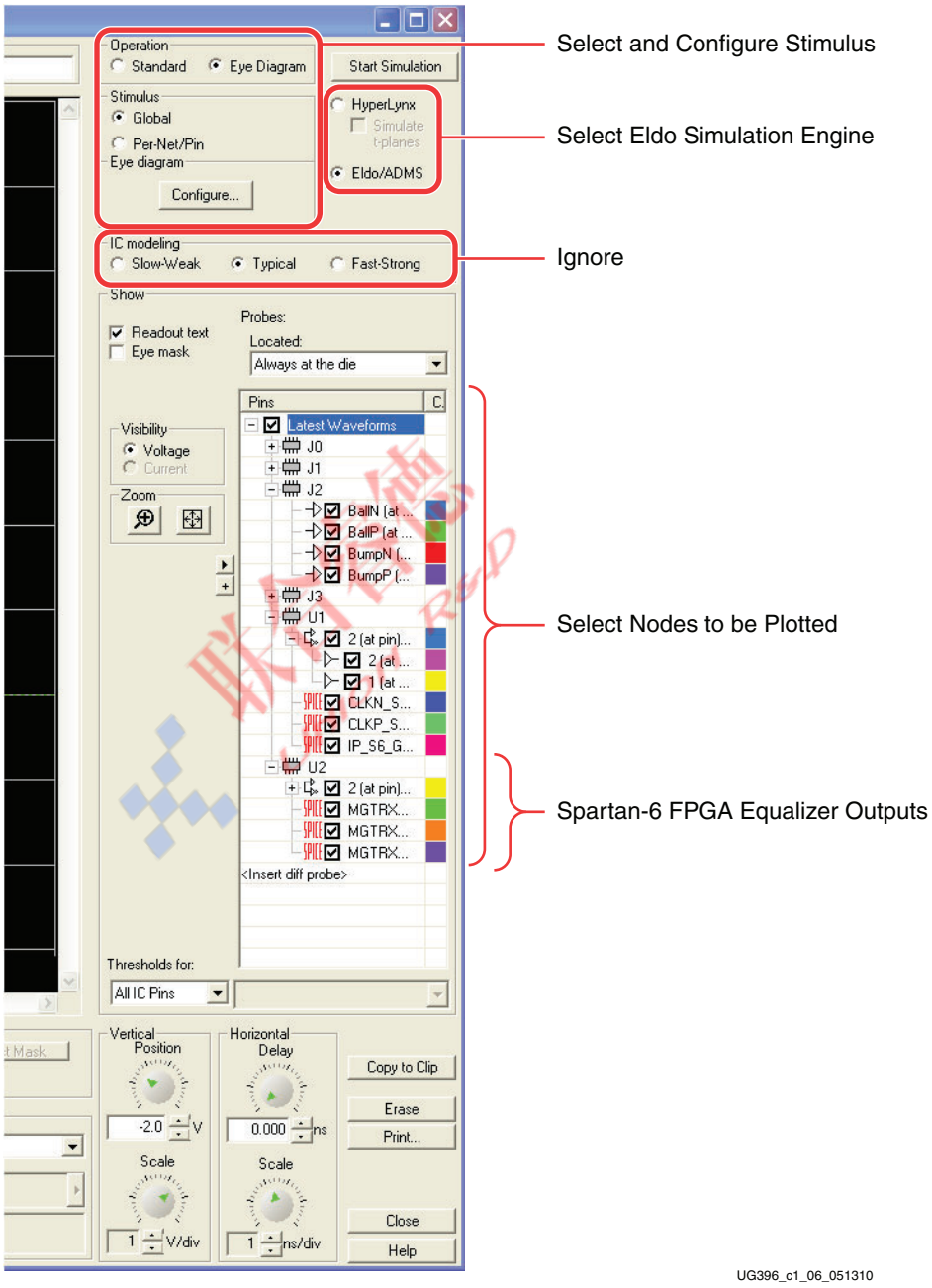

Figure 1-6: **Assign Probes, Select Eldo as Simulation Engine, and Specify Stimulus Type**

3. Add a checkmark to all nodes to plot.
4. Select the type of stimulus for HyperLynx to generate. The oscilloscope has several stimulus waveform options available:
   a. The **Standard** radio button under the **Operation** section provides options to run a single rising or falling edge simulation or a pulse train of a certain frequency and duty cycle.
   b. The **Eye Diagram** radio button under the **Operation** section provides capabilities to set up various bit sequences after the **Configure** button is clicked. The available **Bit Pattern** selection includes **PRBS, 8B/10B, Toggling, USB 2.0**, and **Custom** patterns (see Figure 1-7). The **Configure Eye Diagram** dialog box also allows the user to set up an eye mask for the eye diagram display in the oscilloscope. Refer to the HyperLynx manuals for more details on how to set up these parameters.

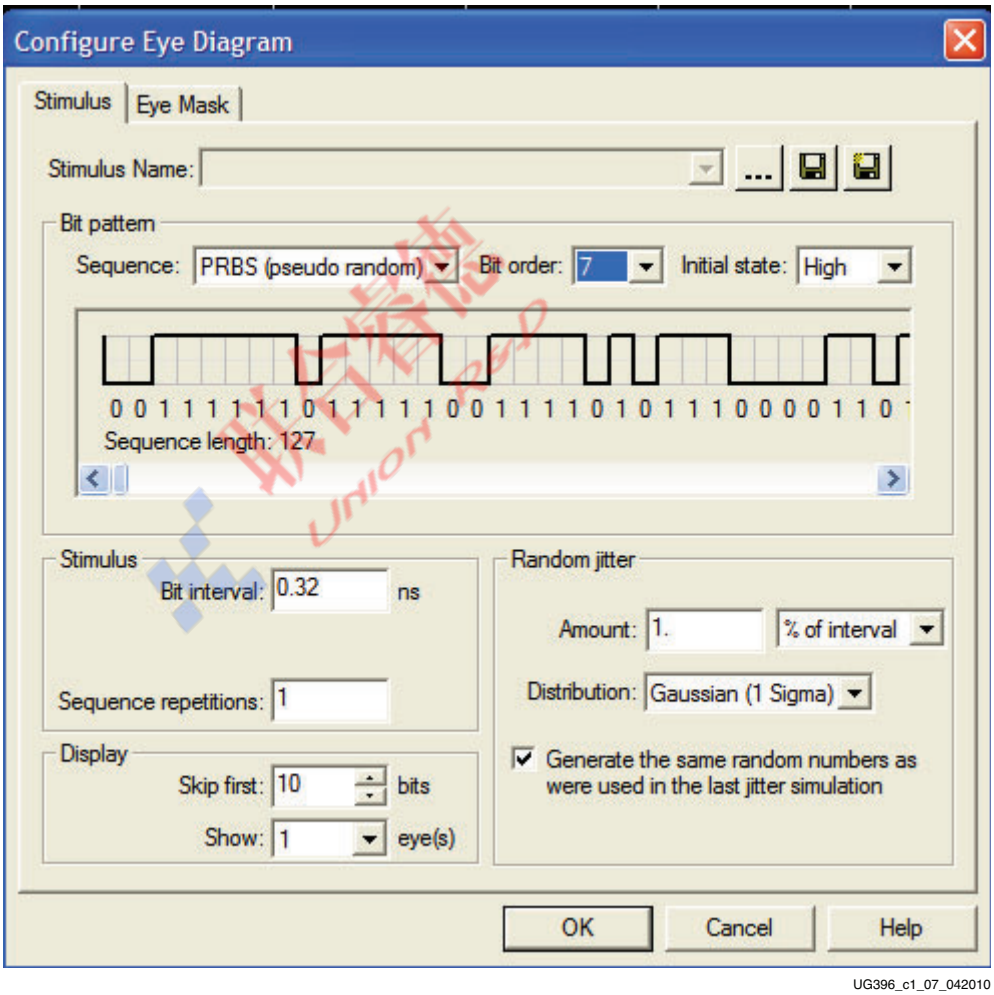

Figure 1-7: **3.125 Gb/s PRBS 7 Stimulus**

Notes relevant to this section:

- The frequency of the pulse train and the time of the bit interval specified in the oscilloscope must match the data rate setting in the TX configurator. Each setting has to be done explicitly.

- The radio buttons in the IC modeling group (Figure 1-6) are ineffective because the simulation corner selections are made using the **Configure Model** button in the **Assign Models** dialog box.
- Checkboxes with the red SPICE label on their left (Figure 1-6) represent schematic symbol nodes that are connected to **NC** in the **Assign Models** dialog box. These nodes are defined on the subcircuit definition line of the symbol. They do not need to be connected to anything else on the schematics because they are used solely to provide probing capabilities for waveforms inside the subcircuits.

Running the Simulation

Click the **Start Simulation** button and wait for the simulator to finish the simulation. The waveform window automatically displays the results for the selected waveforms in the oscilloscope. The vertical and horizontal scales can be adjusted to maximize the waveforms, as shown in Figure 1-8.

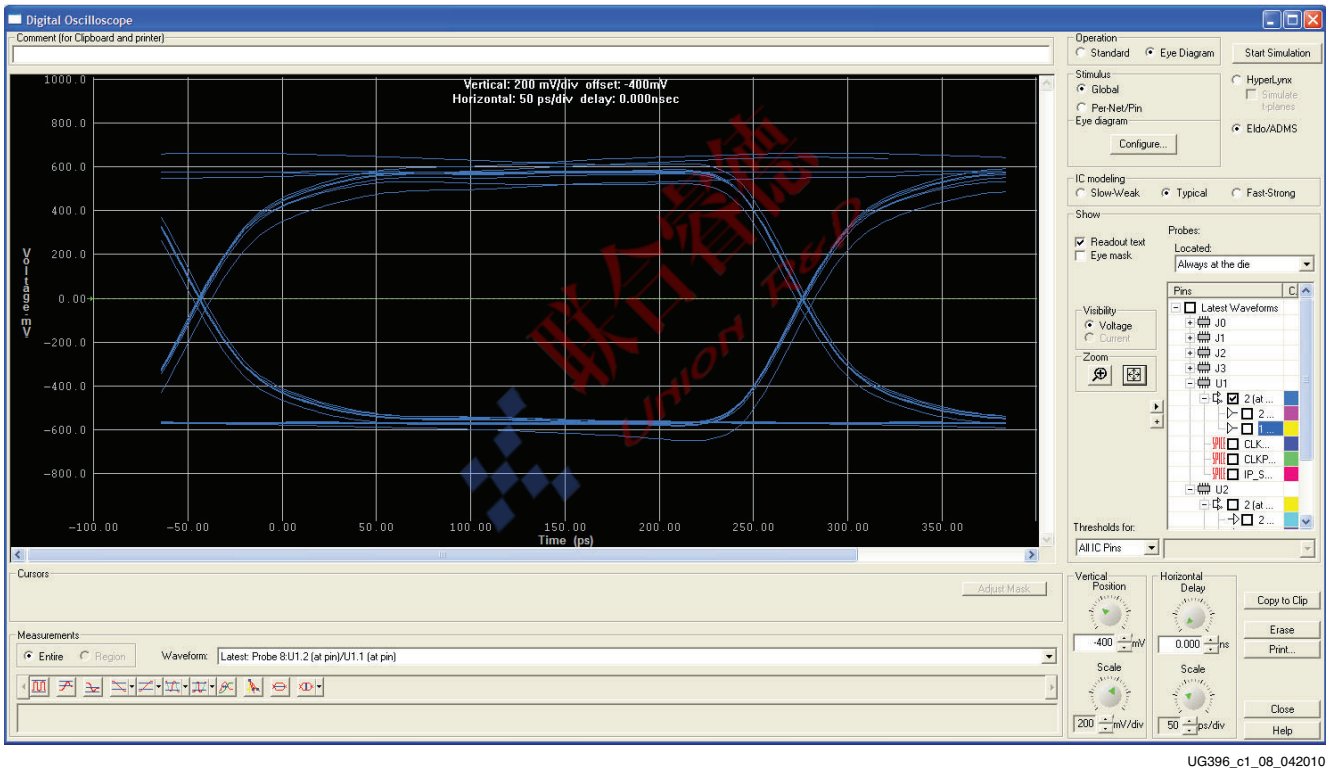

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Figure 1-8: **Example Simulation Results**

Appendix A

Frequently Asked Questions

All Versions

1. What does the "Device-kit .INI file where_am_i\S6_kit.ini does not exist or could not be read" message shown in Figure A-1 mean?

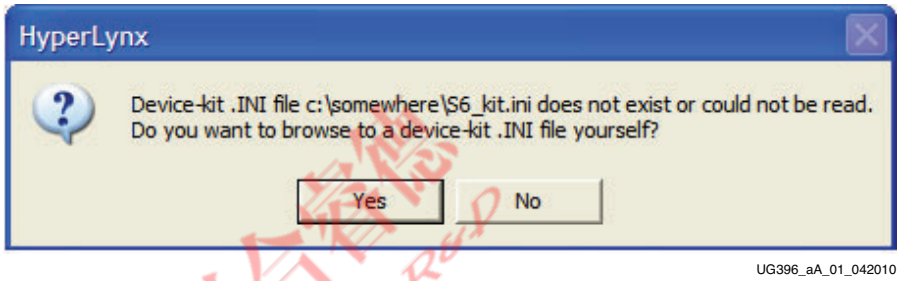

Figure A-1: **Device-kit .INI Error Message**

HyperLynx cannot find the `Device-kit.INI` file, most likely because the `DesignName.pjh` file has an incorrect path for the INI file. The `S6_kit.ini` file is located in the `hl_projects` directory. Either:

- Click **No**, close HyperLynx, edit the PJH file as described in Installation and Requirements, page 7, and start HyperLynx again,

or

- Click **Yes** and browse to the `hl_projects` directory to locate the `DesignName.pjh` file.

2. What is the J0 symbol on the schematic screen (Figure A-2)?

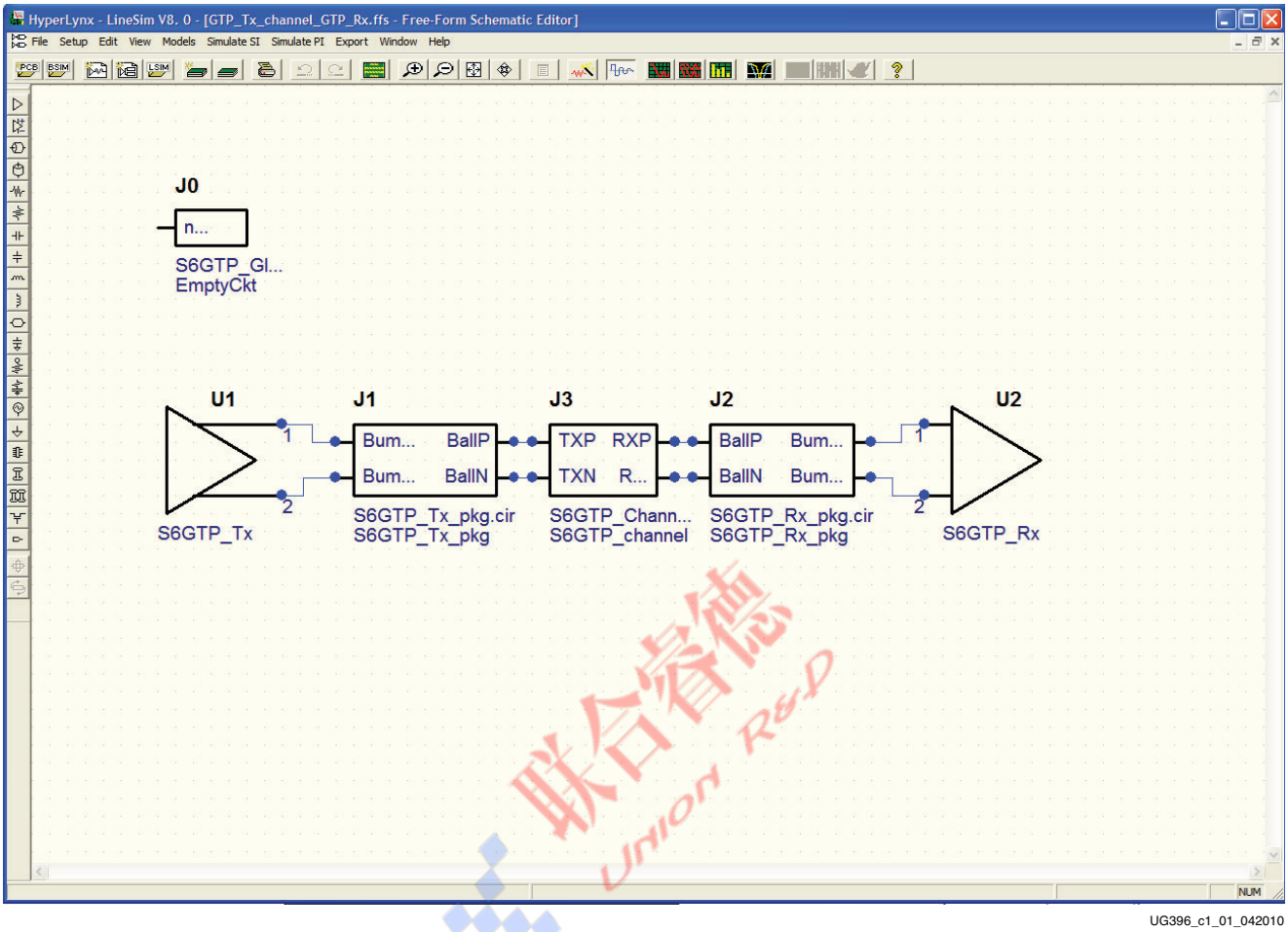

Figure A-2: **J0 Symbol**

The J0 symbol appears unconnected on the schematics screen and must *not* be removed from the schematics. The J0 symbol inserts global simulation parameters, such as **`.TEMP`** and **`.option compat`** (the HSPICE compatibility switch for Eldo) into the project. These parameters are managed automatically by the configurator programs. Removing J0 results in incorrect simulations.

3. What does the "Your model library paths contain at least one space" message shown in Figure A-3 mean?

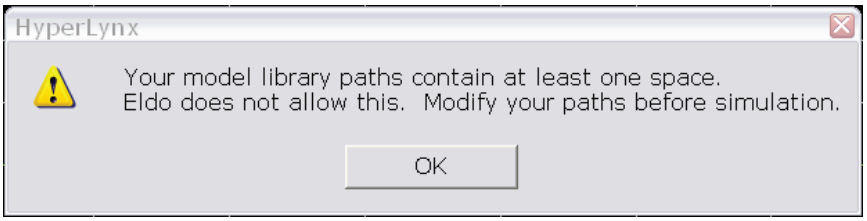

Figure A-3: **Spaces in Path Error Message**

If the installation instructions in Installation and Requirements are followed, this message can usually be ignored. This message appears when model search path directories contain space characters. From the menu bar, select **Setup** → **Options** → **Directories** to verify in the list (Figure A-4) that there are no spaces in the path pointing to the root of this kit.

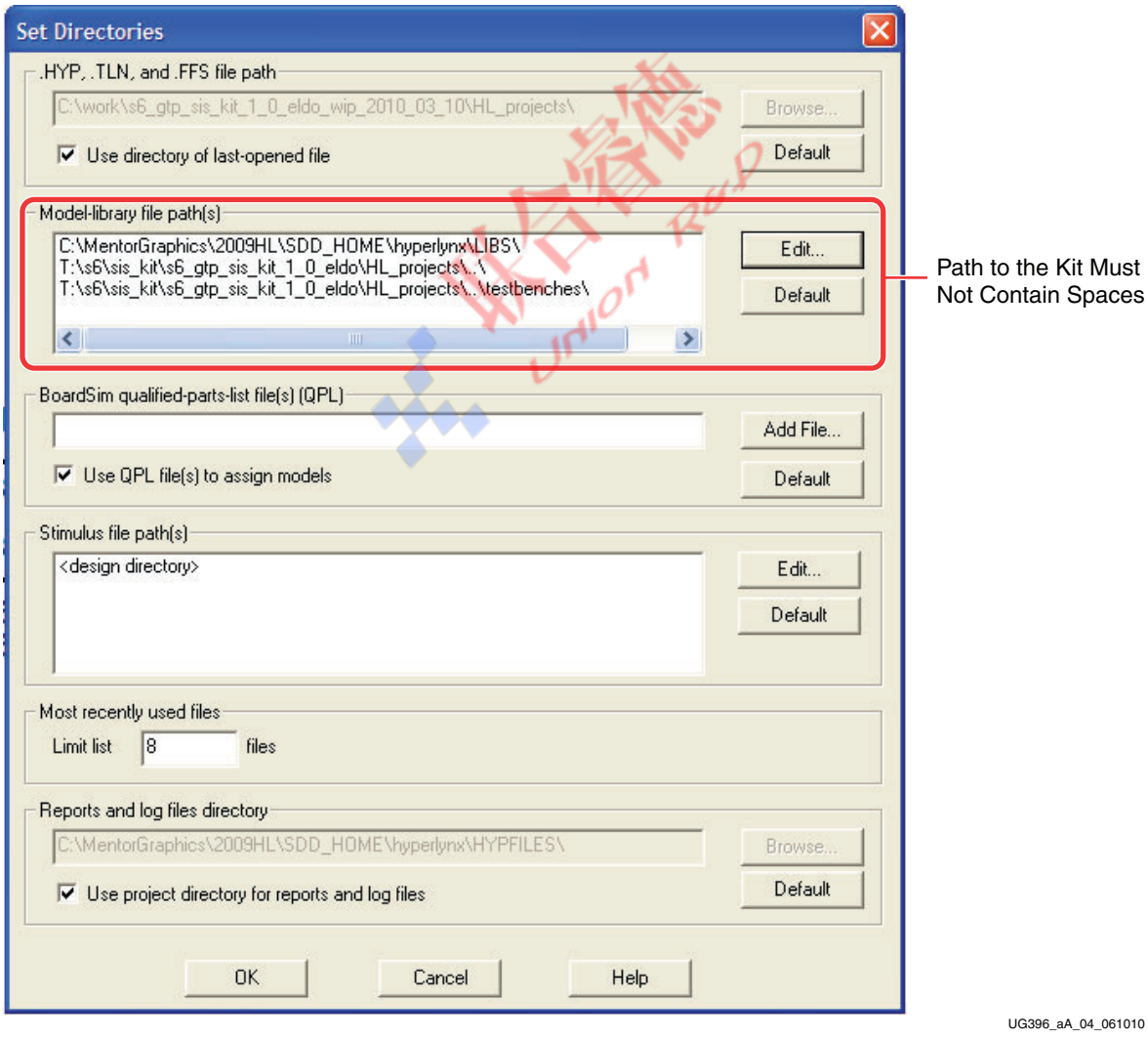

Figure A-4: **Example of Path**

4. What if the simulation does not start or aborts prematurely?

   This might occur if:

   - The correct simulation in HyperLynx is not selected. Verify that Eldo/ADMS is the selected simulator engine in the **Digital Oscilloscope** window.
   - The **HSPICE compatible** radio button is not selected or the Eldo executable is not listed in the **Circuit Simulators** tab of the **Setup** → **Options** → **General** dialog box. See Figure A-5 for proper selection.
   - The HyperLynx license is not set to perform Eldo simulations. Contact the license manager or a Mentor Graphics representative to resolve this issue.

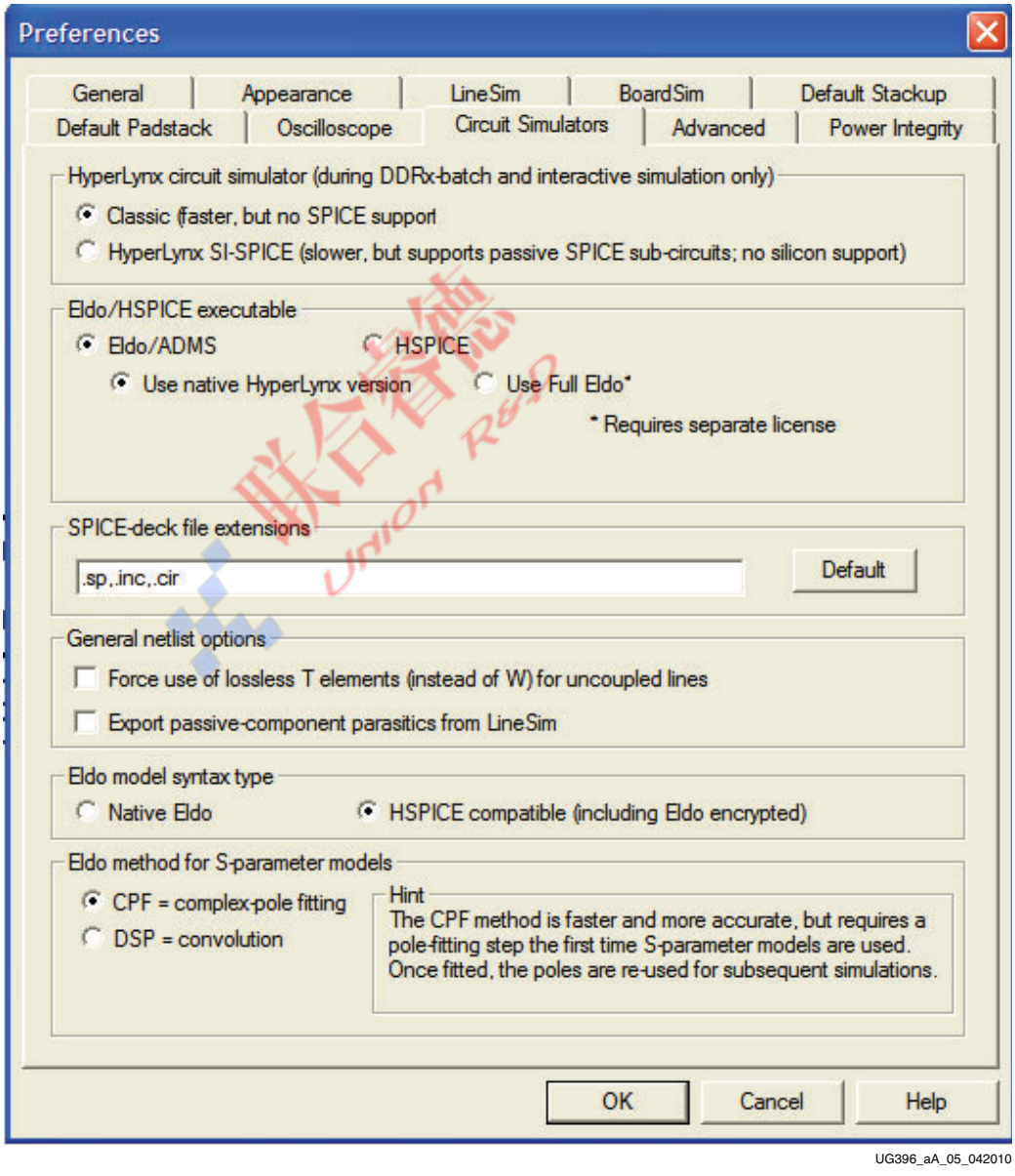

Figure A-5: **HSPICE Compatible Radio Button**

Appendix B

HSPICE and HyperLynx/Eldo Correlation Results

Introduction

The results generated by the HyperLynx and Eldo simulators are validated by executing a set of the same simulations in both simulators and plotting the waveform results on top of each other to verify identical outcomes.

Note: HSPICE version A-2009.03 was used for the S-parameter/circuit correlation and the GTP REFCLK and GTP transceiver simulations.

For this correlation, only the silicon models for the GTP transmitter and receiver are used. Package and channel models are not used, except for the GTP reference clock, where the package model is included.

Table B-1 lists the parameter settings used by the GTP transceiver simulations.

Table B-1: **GTP Transceiver Simulations Parametric Settings**

TXDIFFCTRL	TXPREEMPHASIS	RXEQMIX
Typical Process Corner with Typical Voltage and Typical Temperature		
4'b0000	3'b000	2'b00
4'b0100	3'b000	2'b00
4'b1010	3'b000	2'b00
4'b1010	3'b010	2'b00
4'b1010	3'b100	2'b00
4'b1010	3'b111	2'b00
4'b1010	3'b000	2'b01
4'b1010	3'b000	2'b10
4'b1010	3'b000	2'b11
Fast Process Corner with Maximum Voltage and Cold Temperature		
4'b1010	3'b000	2'b00
4'b1010	3'b011	2'b00
Slow Process Corner with Minimum Voltage and Hot Temperature		
4'b1010	3'b000	2'b00
4'b1010	3'b011	2'b00

The plots are zoomed in and aligned to better highlight the correlation.

These conditions were used for the transceiver correlation:

- A data rate of 3.125 Gb/s
- PRBS7 data pattern
- No external capacitor
- No ground termination

The simulation results are provided in these sections:

- GTP REFCLK Model Correlation, page 23
- GTP Transceiver Model Correlation, page 27

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GTP REFCLK Model Correlation

Figure B-1 through Figure B-3 contain the waveform overlays of the correlation simulations for the GTP REFCLK testbench (`GTP_RefClk.ffs`).

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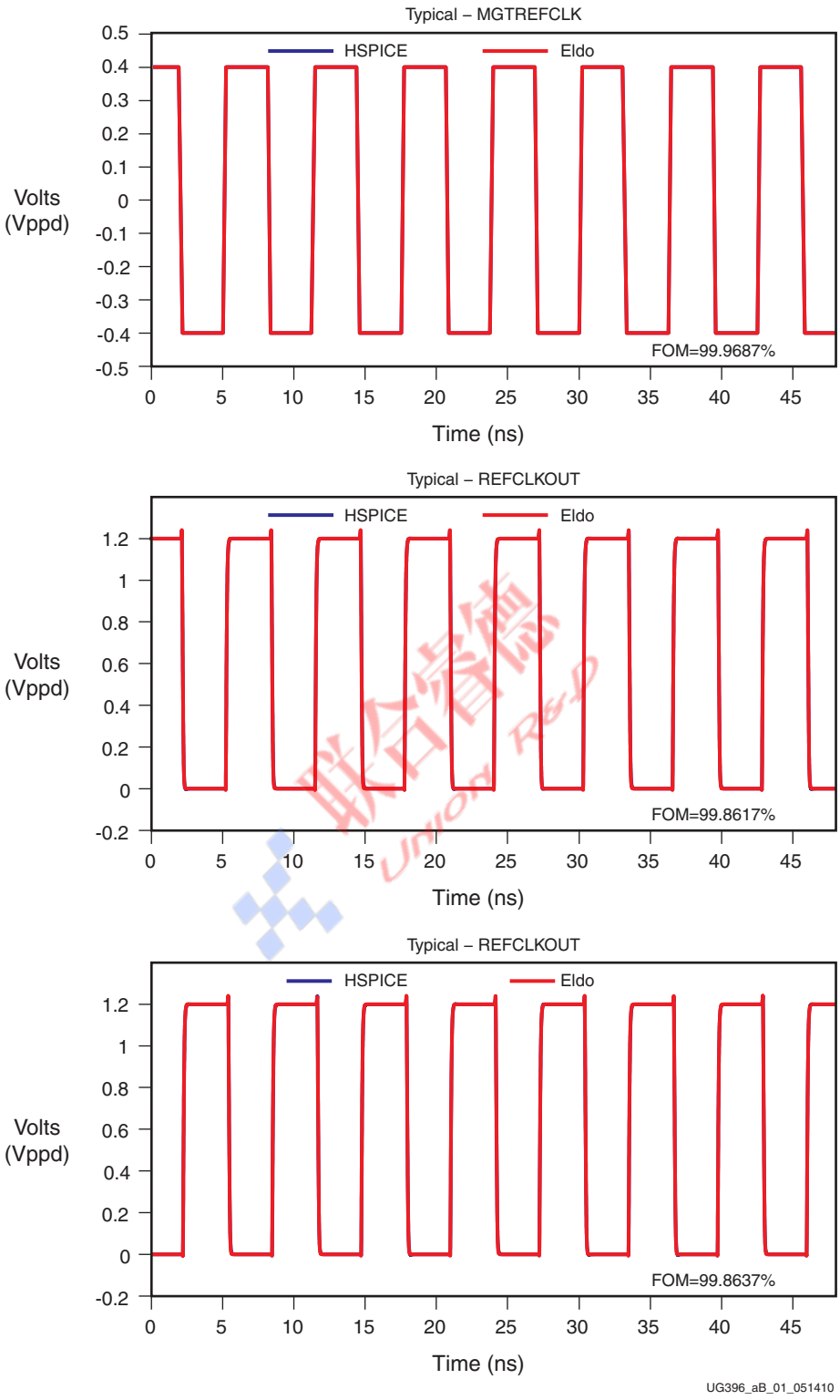

Figure B-1: **GTP REFCLK - Typical**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

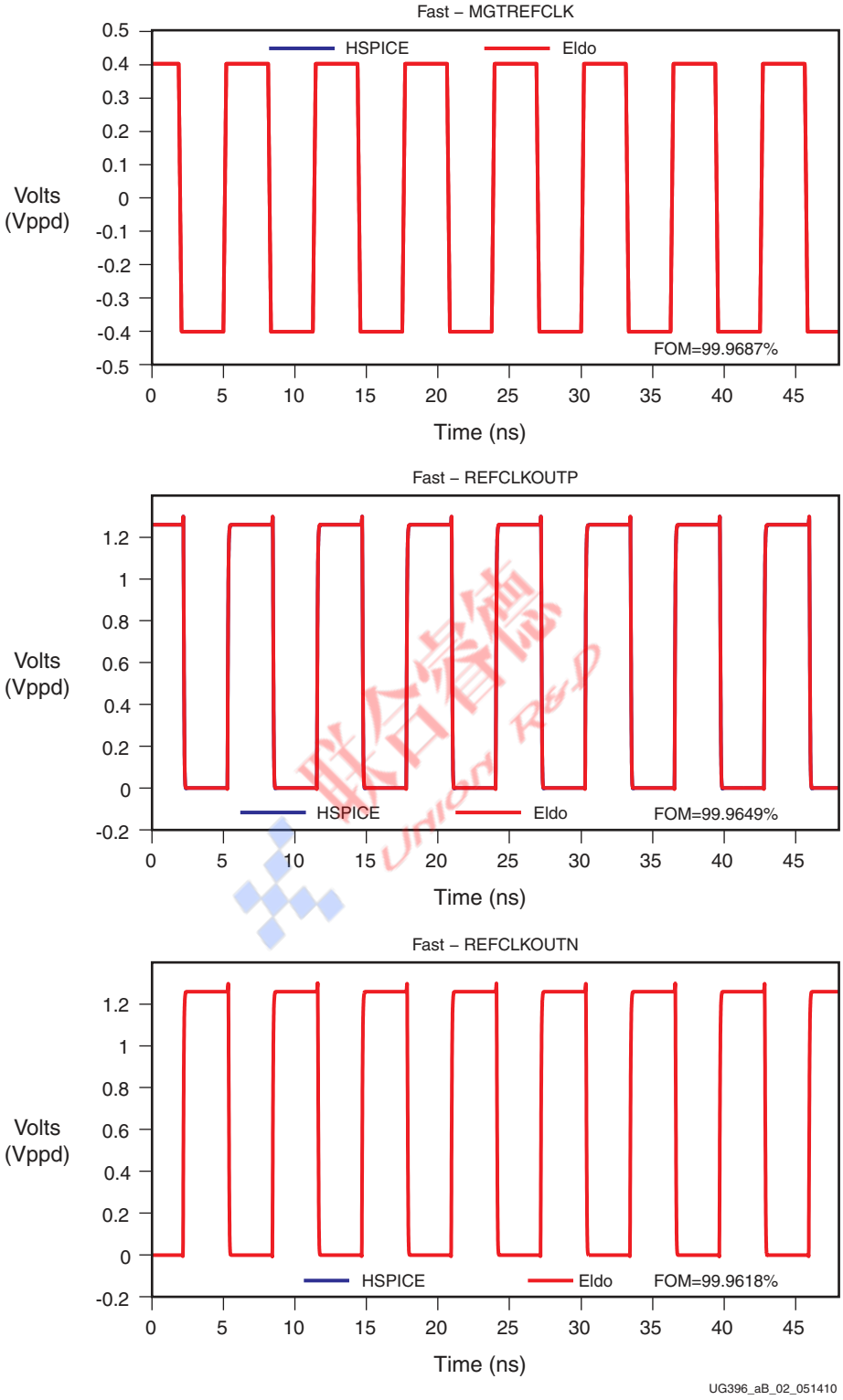

Figure B-2: **GTP REFCLK - Fast**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

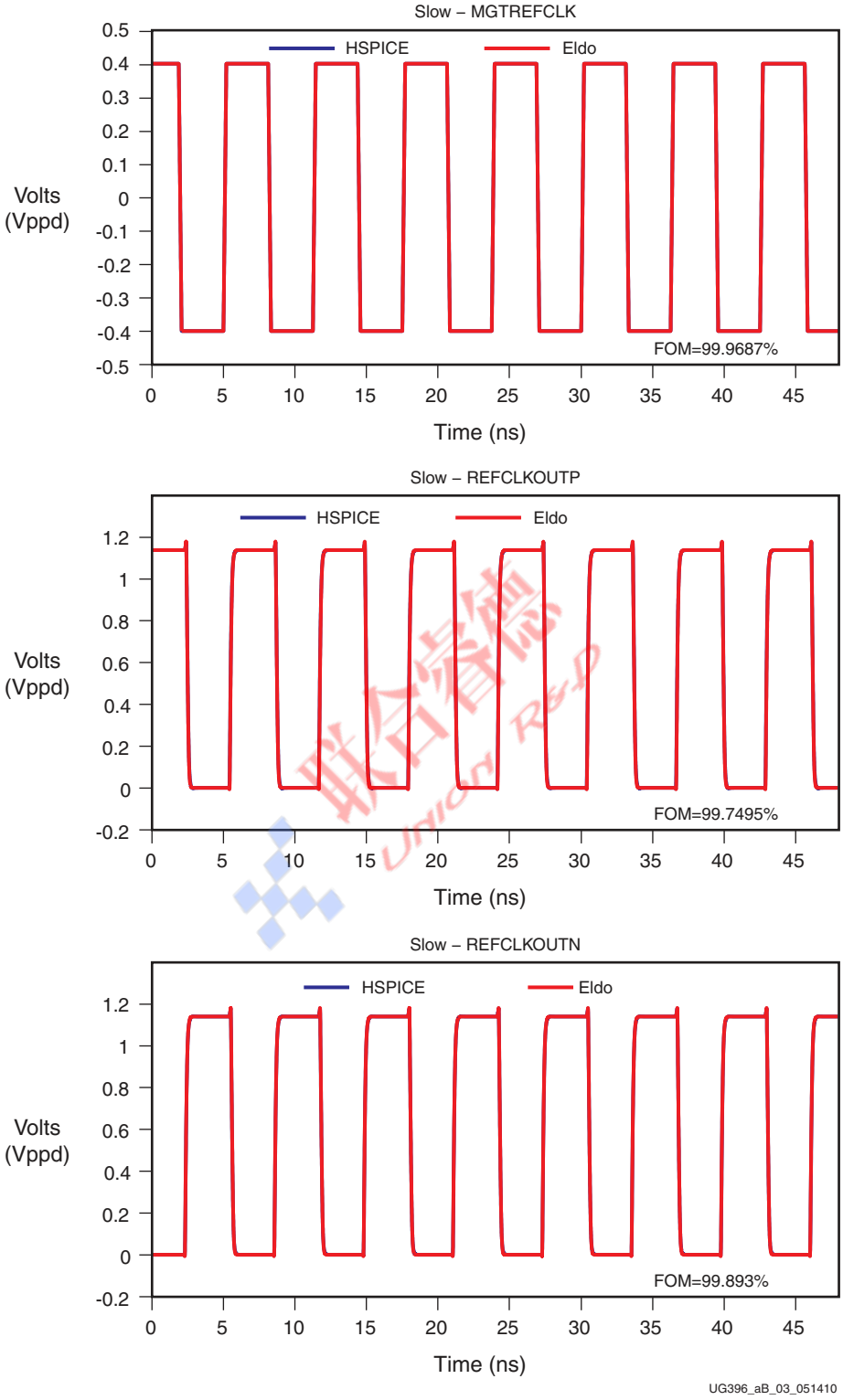

Figure B-3: **GTP REFCLK - Slow**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

GTP Transceiver Model Correlation

Figure B-4 through Figure B-16 contain the waveform overlays of the correlation simulations for the GTP transceiver models.

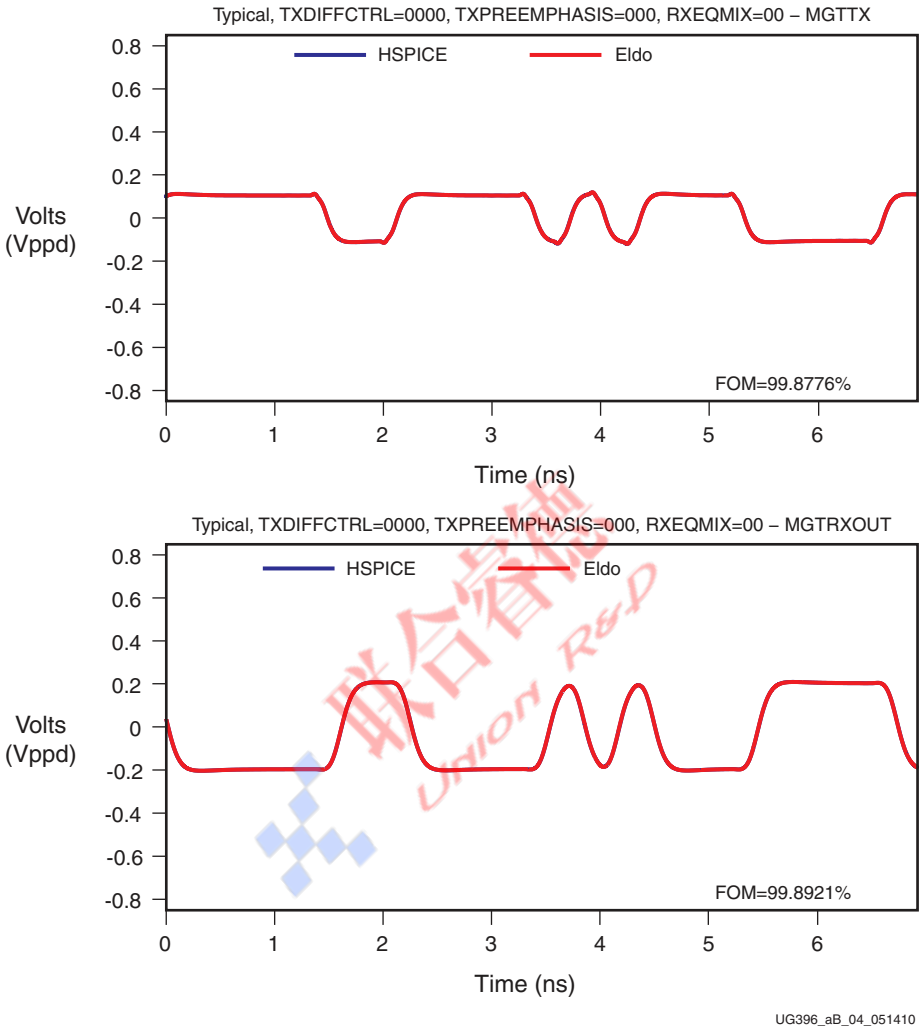

Figure B-4: **TXDIFFCTRL = 0000, TXPREEMP = 000, RXEQMIX = 00 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

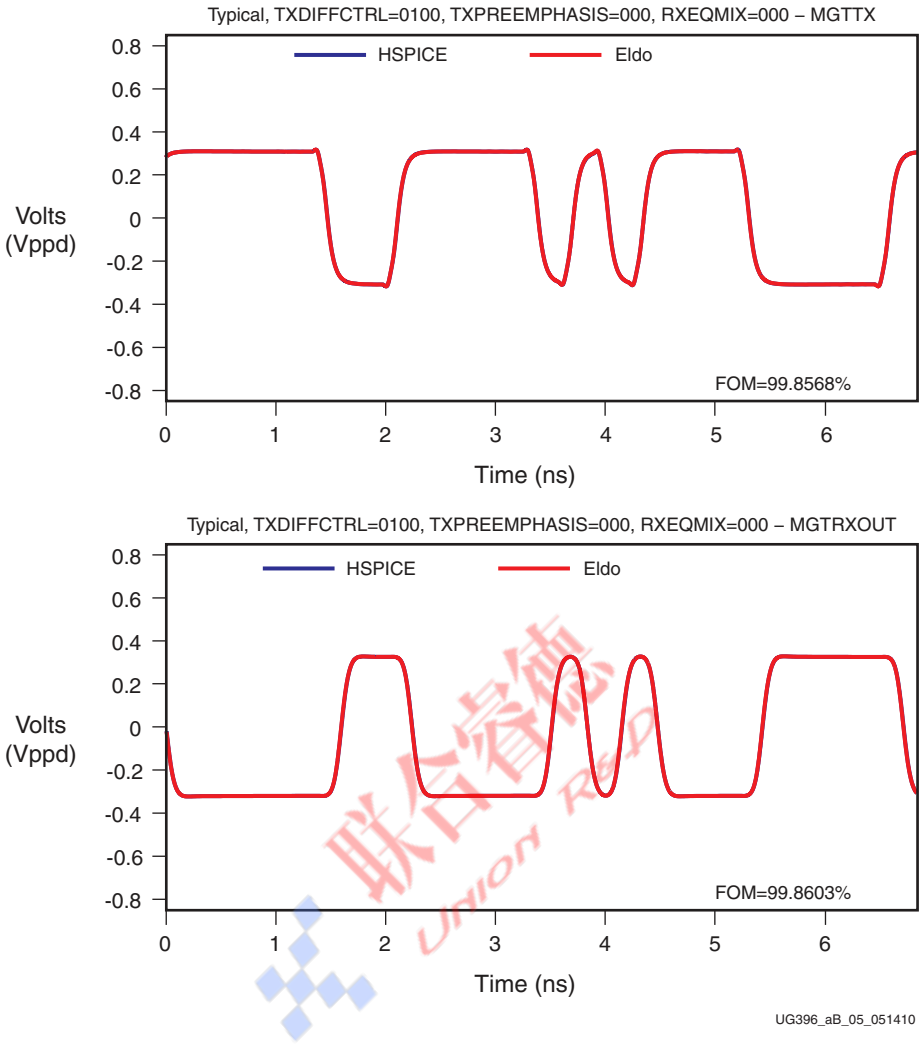

Figure B-5: **TXDIFFCTRL = 0100, TXPREEMP = 000, RXEQMIX = 00 (GTP Transceiver - Typical)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

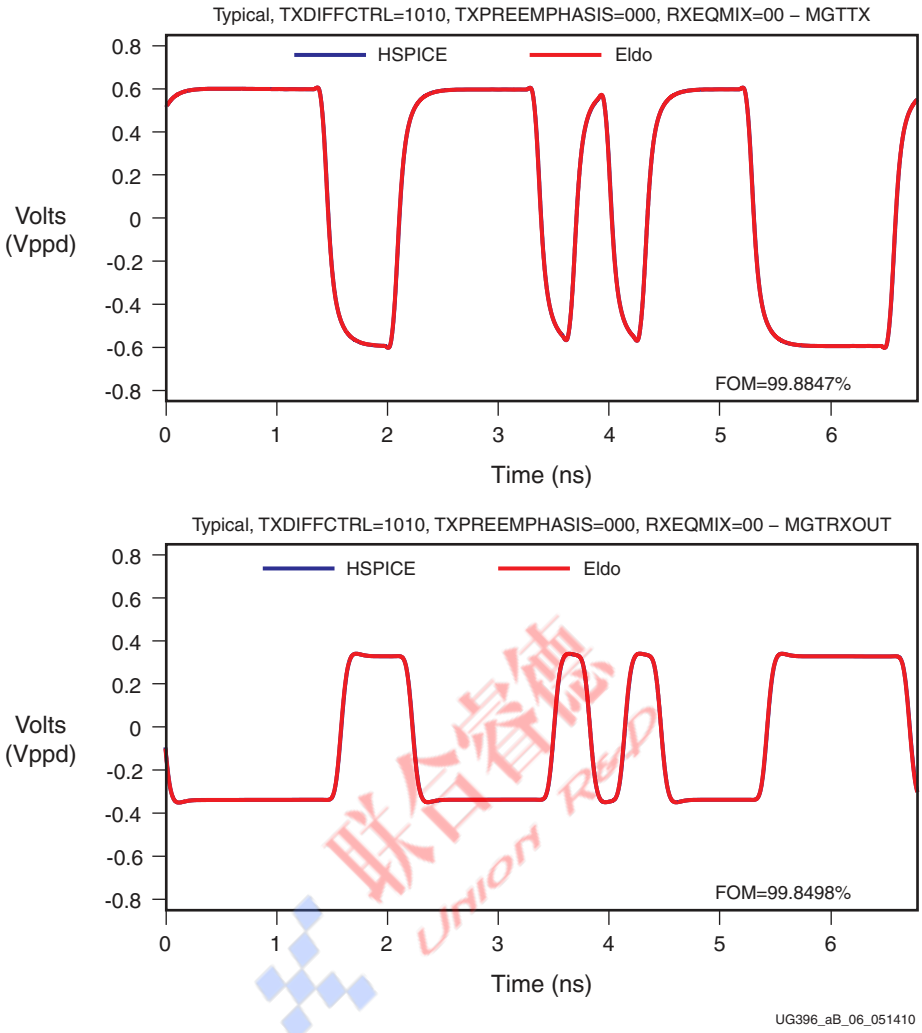

Figure B-6: **TXDIFFCTRL = 1010, TXPREEMP = 000, RXEQMIX = 00 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

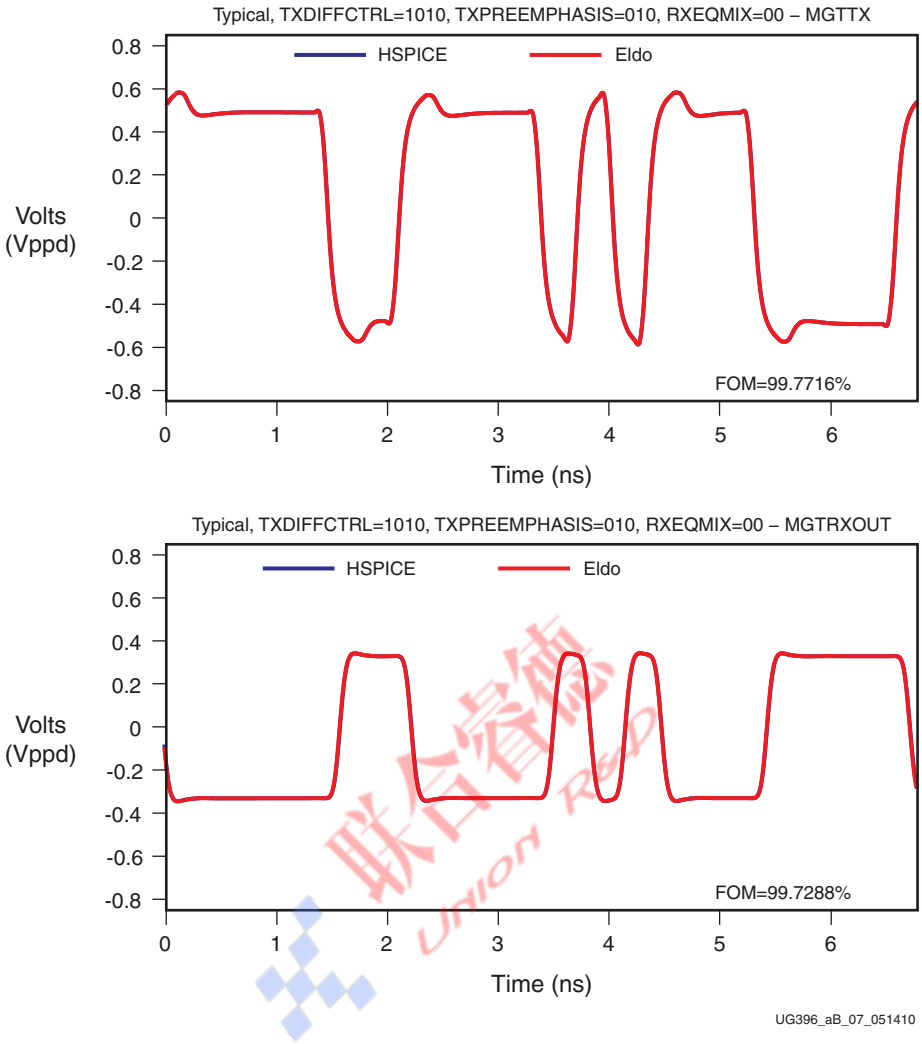

Figure B-7: **TXDIFFCTRL = 1010, TXPREEMP = 010, RXEQMIX = 00 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

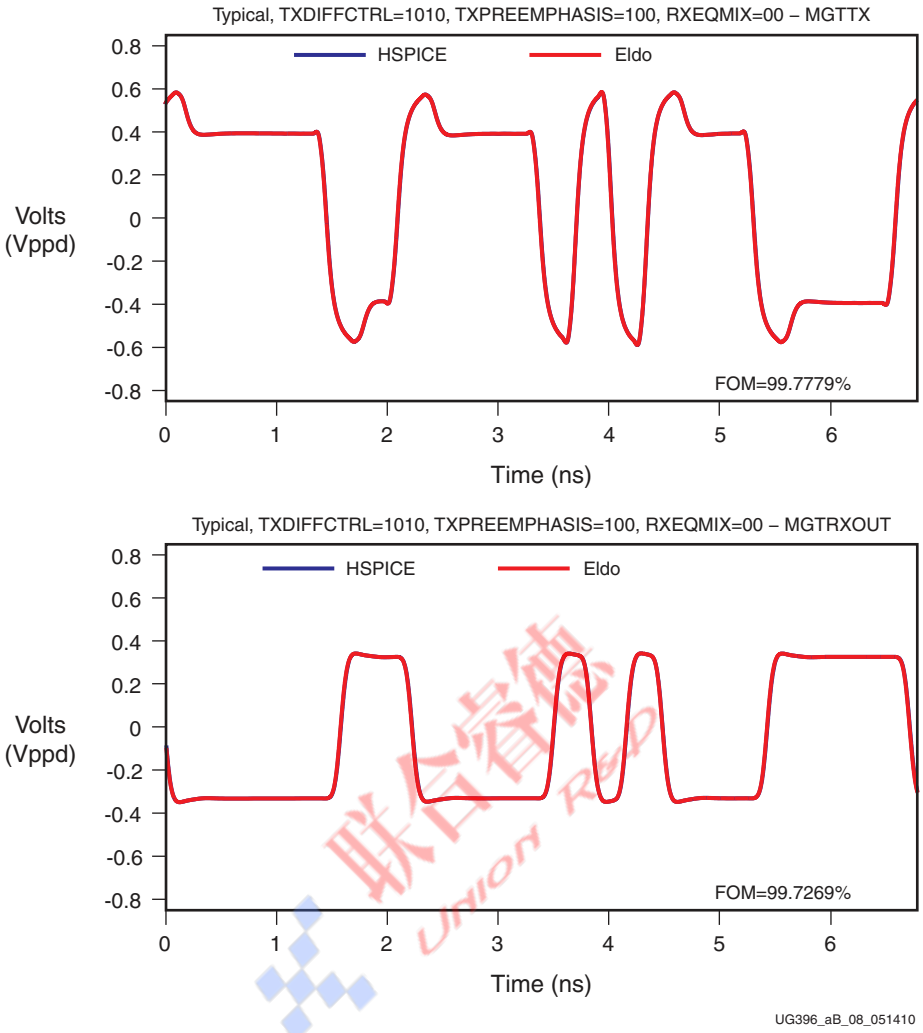

Figure B-8: **TXDIFFCTRL = 1010, TXPREEMP = 100, RXEQMIX = 00 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

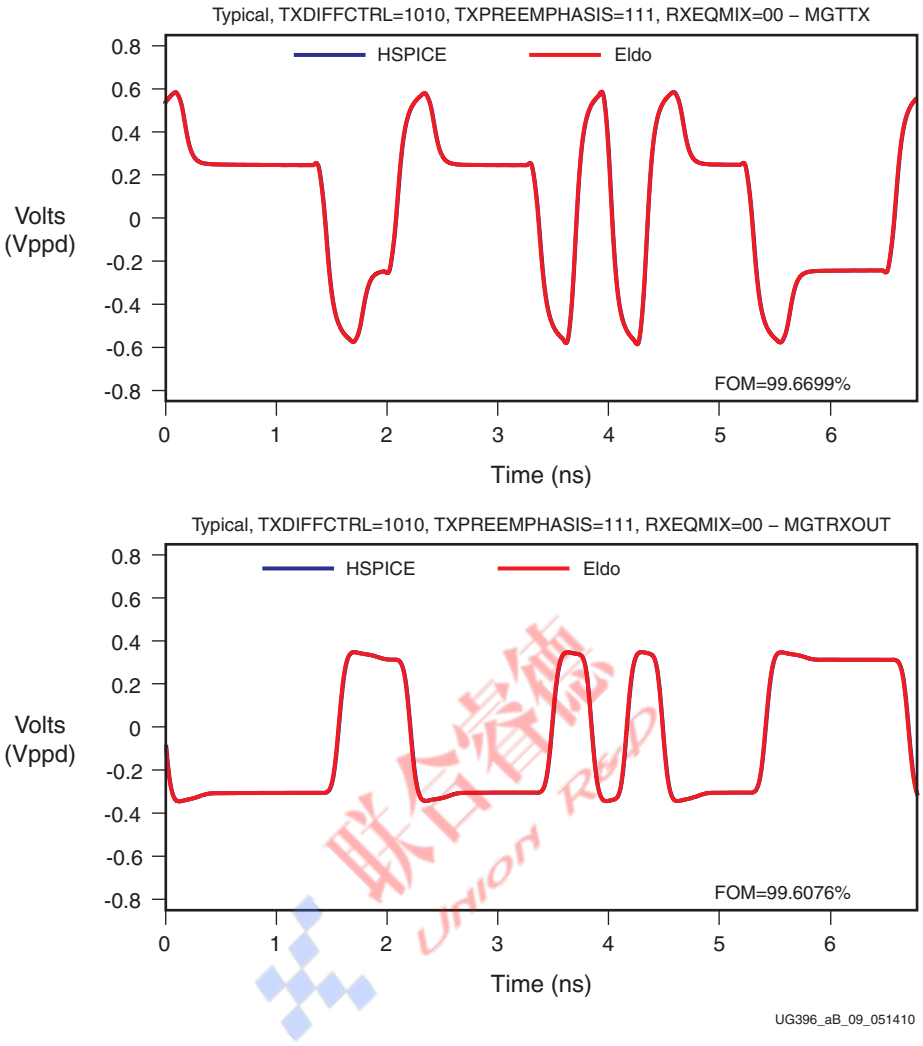

Figure B-9: **TXDIFFCTRL = 1010, TXPREEMP = 111, RXEQMIX = 00 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

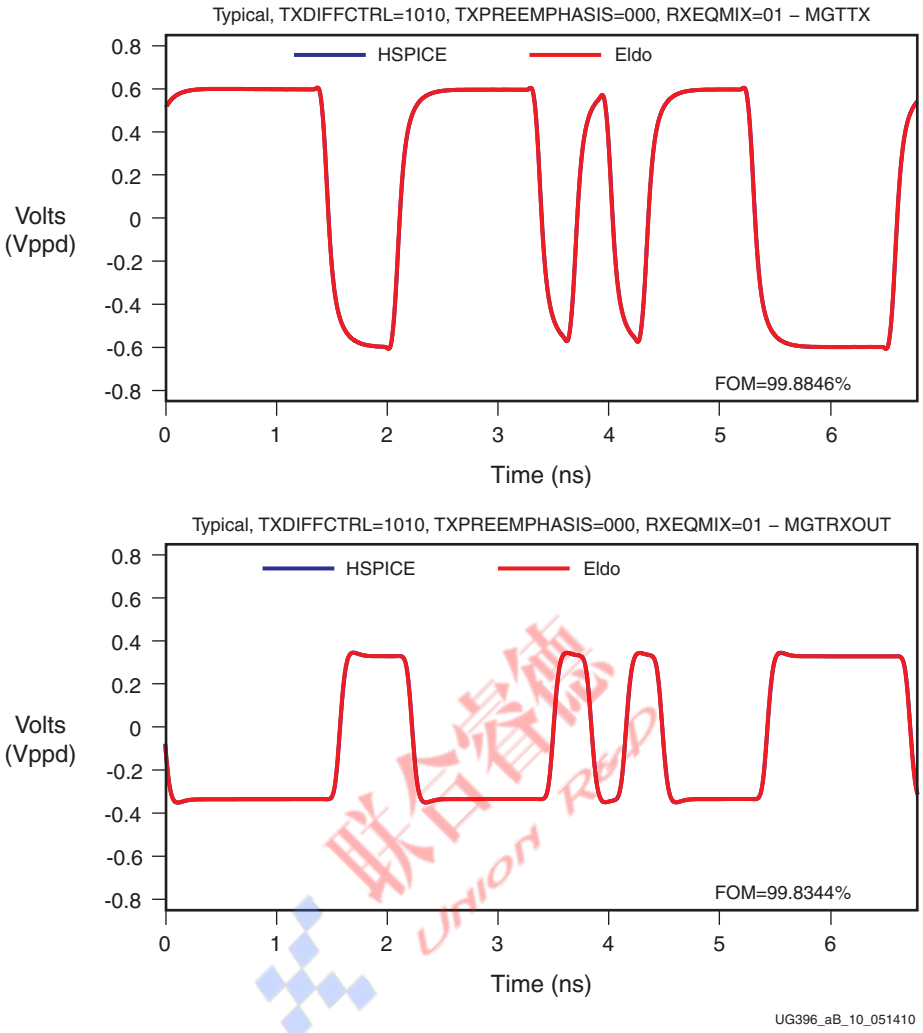

Figure B-10: **TXDIFFCTRL = 1010, TXPREEMP = 000, RXEQMIX = 01 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

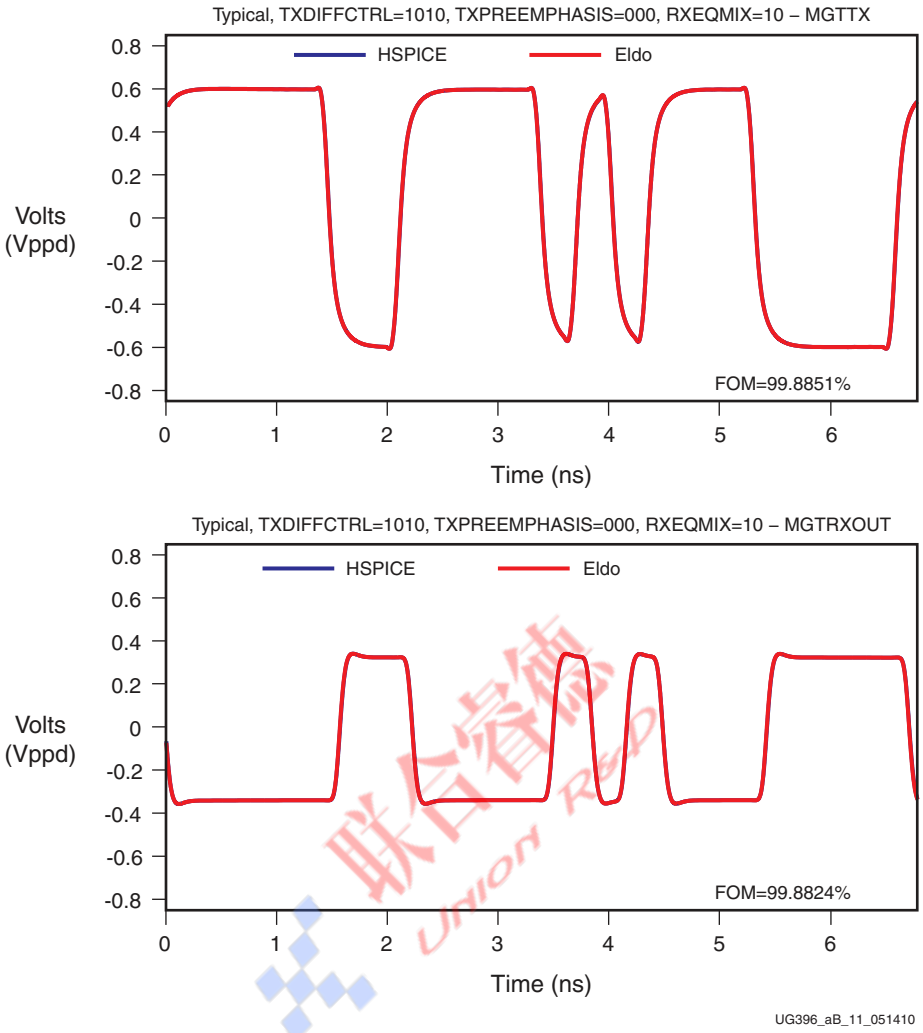

Figure B-11: **TXDIFFCTRL = 1010, TXPREEMP = 000, RXEQMIX = 10 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

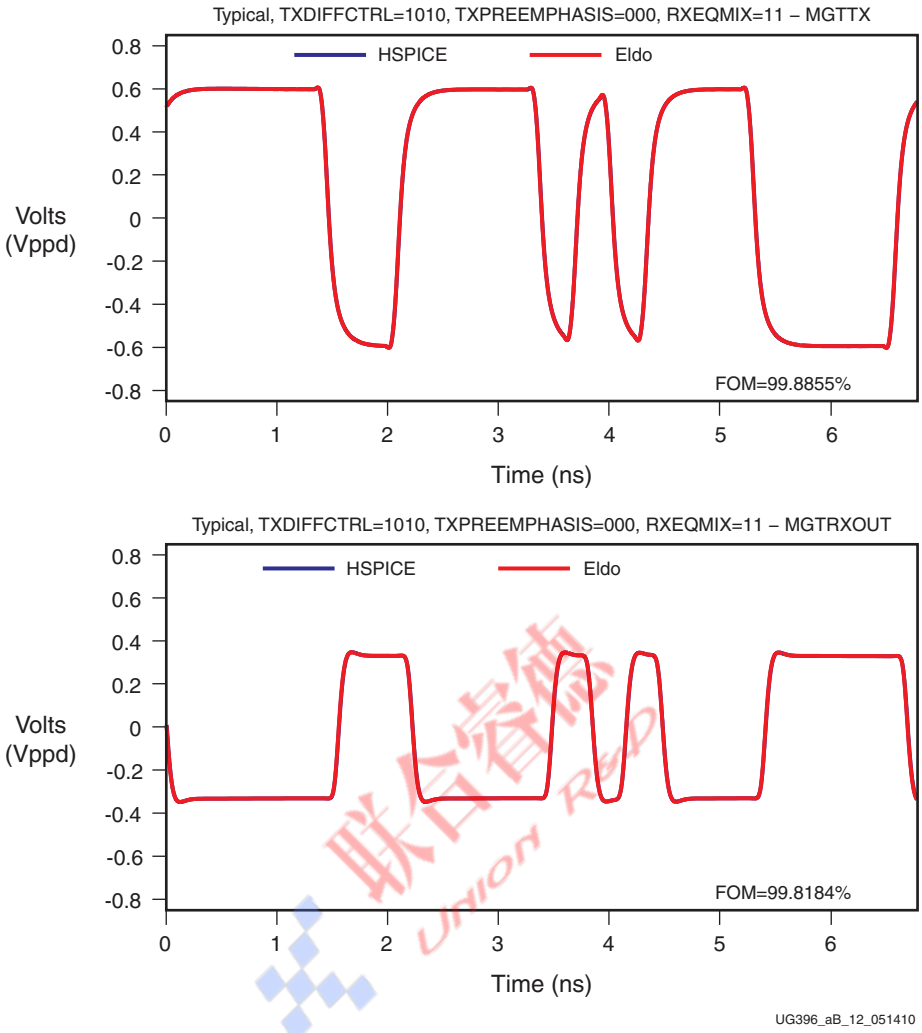

Figure B-12: **TXDIFFCTRL = 1010, TXPREEMP = 000, RXEQMIX = 11 (Typical - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

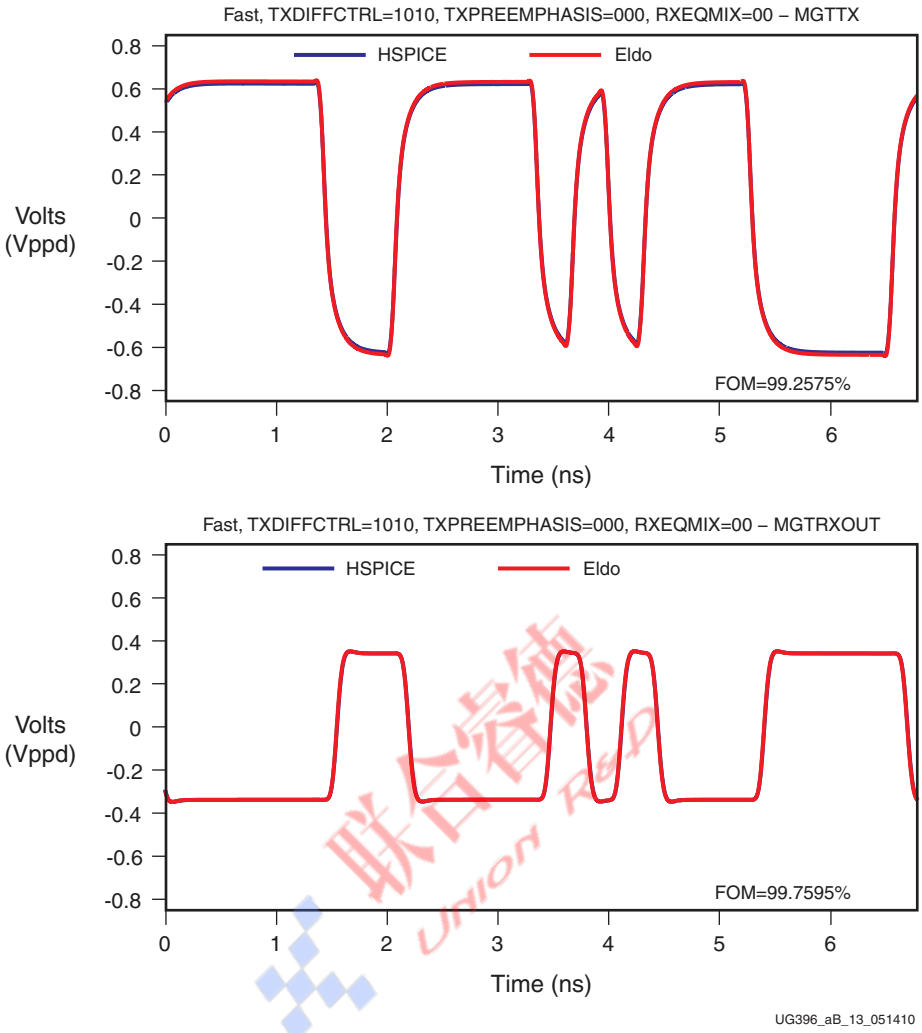

Figure B-13: **TXDIFFCTRL = 1010, TXPREEMP = 000, RXEQMIX = 00 (Fast - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

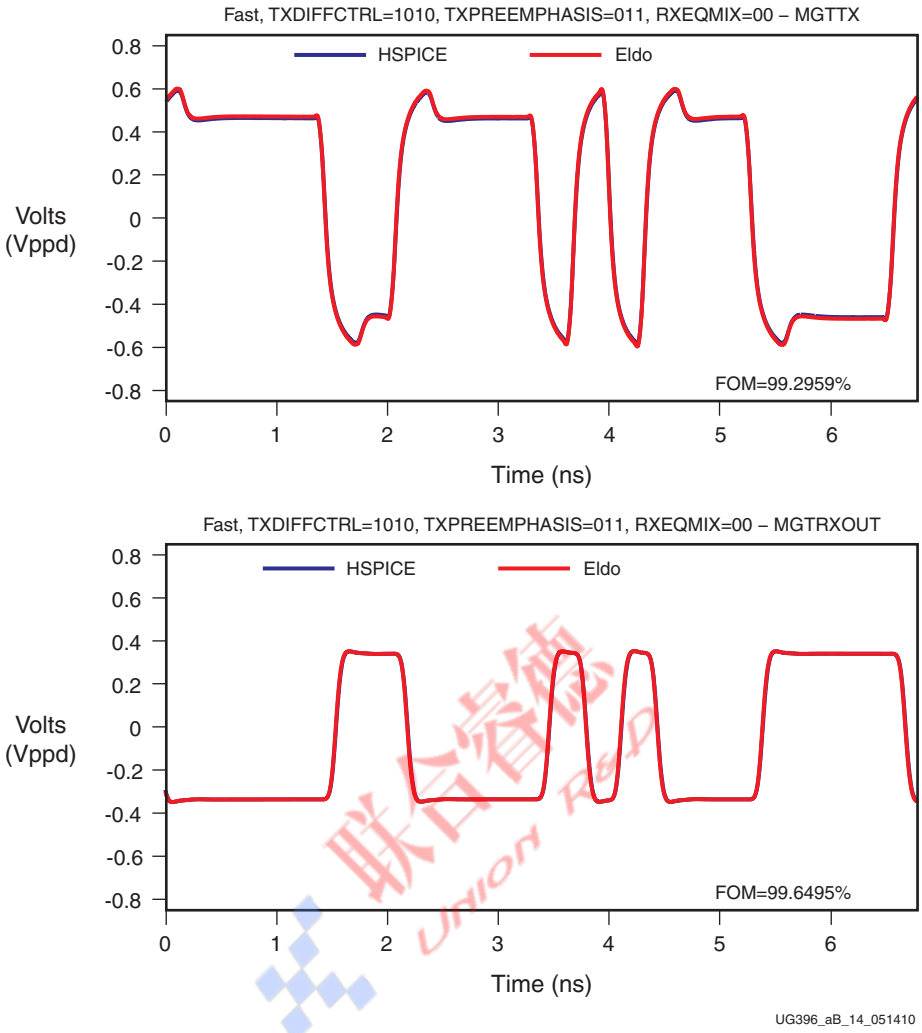

Figure B-14: **TXDIFFCTRL = 1010, TXPREEMP = 011, RXEQMIX = 00 (Fast - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

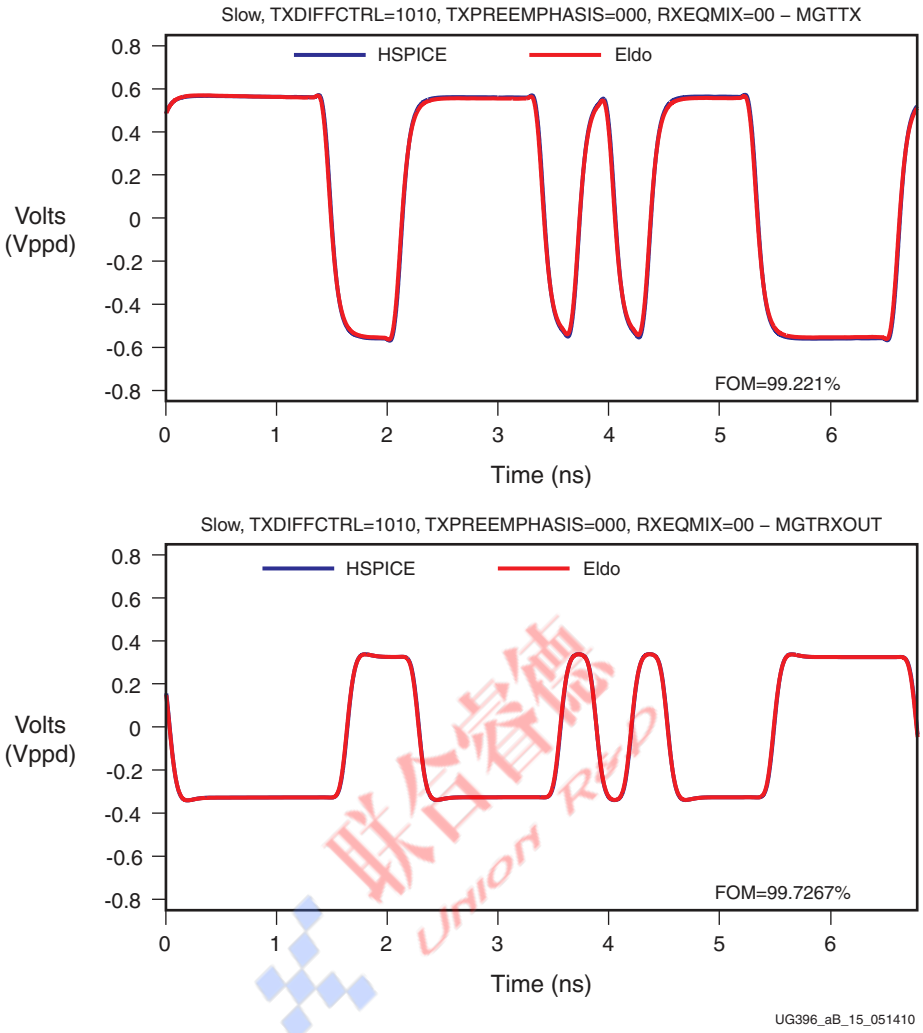

Figure B-15: **TXDIFFCTRL = 1010, TXPREEMP = 000, RXEQMIX = 00 (Slow - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.

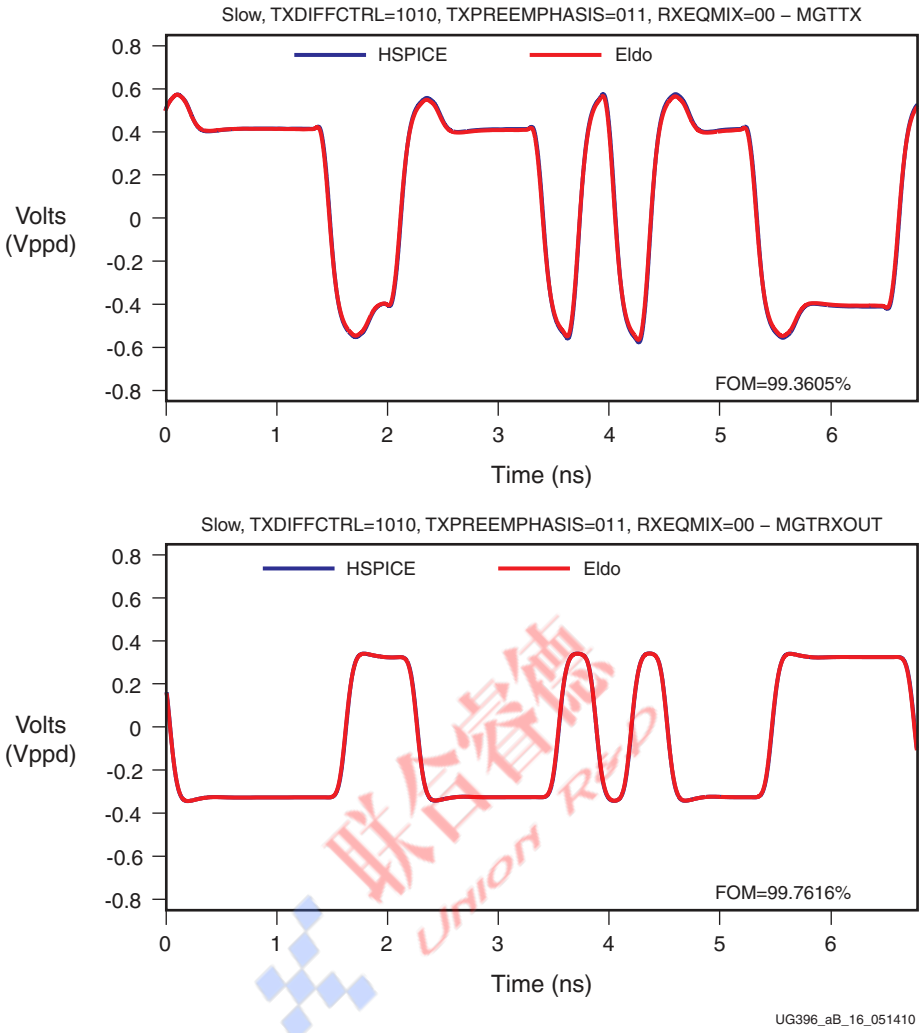

Figure B-16: **TXDIFFCTRL = 1010, TXPREEMP = 011, RXEQMIX = 00 (Slow - GTP Transceiver)**

Note: The blue waveforms cannot be seen because the red waveforms are covering them.